Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

Claims 1 - 10 (canceled):

Claim 11 (currently amended): A semiconducting structure having reduced with soft error rates comprising:

a semiconductor substrate;

a first semiconductor layer over the substrate, said first semiconductor layer being comprised of a first semiconductor material and having a vertical extent defined by an upper extent of the first semiconductor material and a lower extent of the first semiconductor material;

a generally constant electric field across **at least a portion of** the vertical extent of the first semiconductor material, wherein a charge which occurs within the first semiconductor layer is influenced toward the semiconductor substrate; and

a device layer in which a semiconductor device may be fabricated.

Claim 12 (currently amended): The semiconducting structure recited in claim 11 above, wherein the first semiconductor layer over the substrate further comprises a graded dopant concentration **over the at least a portion of the vertical extent of the first semiconductor material**, said graded dopant concentration having a first dopant concentration established at the lower extent of the semiconductor material, a second dopant concentration established at the upper extent of the semiconductor material and a

plurality of dopant concentrations between said first dopant concentration and said second dopant concentration **over the at least a portion of the vertical extent of the first semiconductor material, and** between the upper extent and lower extent of the first semiconductor material.

Claim 13 (original): The semiconducting structure recited in claim 12 above, wherein said second dopant concentration is based on said semiconductor device to be fabricated in the device layer.

Claim 14 (original): The semiconducting structure recited in claim 12 above, wherein said device layer is formed within the vertical extent of first semiconductor material.

Claim 15 (original): The semiconducting structure recited in claim 13 above further comprises:

a second electric field formed at the lower extent of the first semiconductor material.

Claim 15 (original): The semiconducting structure recited in claim 15 above, wherein the second dopant concentration is based on a dopant concentration of said semiconductor substrate, wherein said second dopant concentration is different from said dopant concentration of said semiconductor.

Claim 16 (original): The semiconducting structure recited in claim 13 above further comprises:

a second electric field below the first semiconductor material.

Claim 18 (original): The semiconducting structure recited in claim 17 above, wherein said semiconductor substrate is a P+ semiconductor substrate, and said semiconducting structure further comprises:

an undoped intrinsic layer formed over said P+ semiconductor substrate and under said first semiconductor layer.

Claim 19 (currently amended): The semiconducting structure recited in claim 17 above, wherein said semiconductor substrate is a P- semiconductor substrate, and semiconducting **structure** further comprises:

a buried n-layer formed over said P- semiconductor substrate; and

an undoped intrinsic layer formed over said buried n-layer and formed under said first semiconductor layer.

Claim 20 (original): A method for fabricating recited in claim 11 above, wherein the first semiconductor layer is an epitaxial first semiconductor layer.